10/813,240

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Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date
YH	AA	4,675,845	6/87	Itoh, et al.	365	51	
YH	AB	4,389,715	6/83	Eaton, Jr., et al.	365	200	
YH	AC	4,727,516	2/88	Yoshida, et al.	365	200	
YH	AD	4,648,075	3/87	Segawa, et al.	365	200	
YH	AE	4,837,747	6/89	Dosaka, et al.	365	200X	11/30/97
YH	AF	5,265,055	11/93	Horiguchi, et al.	365	200	10/10/89
YH	AG	5,617,365	4/97	Horiguchi, et al.	365	200	10/10/89
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YH	AJ	4,752,914	06/88	Nakano et al	365	200	
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Examiner Initial		Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No
YH	AM	60-130139	11/85	Japan				X
YH	AN	62-40700	2/87	Japan			X	
YH	AO	59-135700	8/84	Japan			**	
	AP			**see listing AH above				
	AQ							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

YH	AR	IEEE Journal of Solid-State Circuits, Vol. SC-16, No. 5, October 1981, pp. 479-487.
YH	AS	IEEE PROC., Vol. 130, Pt. I, No. 3, June 1983, pp. 127-135.
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YH	AU	IEEE Journal of Solid-State Circuits, Vol. 26, No. 1, January 1991, pp. 12-17.
YH	AV	"System for Efficiently Using Spare Memory Components for Defect Corrections Employing Content-Addressable Memory," IBM Technical Disclosure Bulletin, vol. 28, no. 6, November 1985, pp. 2562-2567.

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	7/23/04